cadence

PSpice vs. Free Board Level Analog Simulator

Feature Comparison Matrix

	Free Simulator	PSpice® Technology
Libraries and Modeling		
Models	Primarily LT device	Several leading device and component manufacturers
Simulation model shipped with installation	~2000 models	~34000+ models
Model editing and new model creation		●
Modeling apps		●
Devices		
Advanced magnetics		●
IGBT		●
True digital primitives		●
RAM/ROM		●
GaAsFET Model - TOM-2 and TOM-3		●
Coupled transmission line		●
Jiles-Atherton magnetic core model		●
Simulation		
Solvers	Multiple	Multiple
Automatic convergence diagnostic and resolution tool		●
Advanced convergence aids	Limited capability	Exhaustive
Checkpoint/restart		●
Resume/continue mode		●
Accuracy vs. speed trade-off	Limited capability	Automated - SPEED dial
User-defined functions	●	●
Assertions		●
Simulation manager - schedule/manage set of simulations		●
Waveform Analysis		
Axis settings	Limited capability	Exhaustive
Support multiple trace plot as one (plot template)		●
Support text and waveform labeling		●
Performance analysis		●
Plot histogram		●
Perform measurement with waveform analysis		●
Post-analysis measurement		
Cursor support for multiple traces/plot	Limited capability	●
Pre-configured, commonly used one-click cursor navigation		●
Waveform arithmetic	●	●
User-defined expression/macro	●	●
Export simulation result	●	●
Create stimulus from simulation result		●
Ability to plot B-H curve		●
Hysteresis core loss calculation		●
Marching waveform	●	●
Compare different simulation results - one on top of other		●
Read data from oscilloscope		●
Ability to annotate operating point result on schematic		●
Support for scripting language (Tcl)		●

	Free Simulator	PSpice® Technology
Encryption		
Basic	●	●
AES		●
DES		●
Personal key-based encryption		●
Mixed-Mode Simulation		
Event-based simulator		●
Ability to model timing characteristics of digital devices		●
Ability to model I/O characteristics of digital devices		●
Programmable logic arrays		●
Random access memory		●
Tri-state gates		●
Digital stimulus		●
Logic expression		●
Pin-to-pin delay		●
Constraint		●
EDGE and level-triggered devices		●
SETUP/HOLD timing		●
Auto insertion of AtoD and DtoA devices		●
Design and Modelling Utilities		
Model Editor - extract model parameter from datasheet curves		●
Stimulus Editor		●
Magnetics design, modeling, and manufacturing		●
Categorized libraries		●
Search based on parametric data of devices		●
Report generation		●
Schematic Capture		
Multi-sheet design		●
Symbol generation	Limited capability	Comprehensive wizard-based approach
Archive project		●
Integrated SI simulation environment		●
Integrated PCB tools		●
Integrated component information system solution/flows		●
Design reuse (start a new design from existing design)		●
In-schematic modeling	Very limited	●
System Design Capability		
Integration with MATLAB - Simulink		●
Goal-based circuit optimization		●
Waveform-based circuit optimization		●
Sensitivity analysis		●
Analog worst-case analysis		●
Digital worst-case timing analysis		●
C/C++ based model development and simulation		●
Verilog-A model simulation		●
Stress analysis (SMOKE)		●
Heat sink simulation and component deration design		●
Design space exploration		●
Monte Carlo analysis	Limited	●
Miscellaneous		
Learning module		●
Design template for most commonly used circuits		●
Design examples	●	●
Help	Limited - only offline	Exhaustive, both online and offline
Support	Small R&D team with limited support	●
Updates	Unplanned	Regular and has predictable schedule