OrCAD PCB Designer Features Comparison:
PCB Designer 'Standard' (PO3005) vs 'Professional' (PO3010)
(ECADtools, October 21, 2018)

Schematic Capture	Standard	Pofessional
Schematic Entry & Data Management		
Graphical, flat and hierarchical page editor and picture block hierarchy	✓	✓
PSpice Mixed Signal Analysis - LITE version (limited to 75 nodes)	✓	✓
Net Groups - Complex bus definition	✓	✓
AutoWire	✓	✓
44,000 Schematic symbols	✓	✓
Coloured Components / nets	✓	✓
Tcl TK scripting support	✓	✓
Online design rule check including custom DRC capability and Waive DRC	✓	✓
Forward and back-annotation of properties / pin-and-gate swaps	✓	✓
Schematic Part and Library editor	✓	✓
Custom Symbol Creator & Editor	✓	✓
Cross-probing and cross-placing	✓	✓
FPGA design-in / pin import & export	✓	✓
Multiple PCB netlist interfaces	✓	✓
Digi-Key (PartLink App) Component Parametric data directly from web	✓	✓
Property editor for pins, components, nets	✓	✓
OrCAD SigXplorer SI Analysis	✓	✓
Advanced Annotation	✓	✓
Design Compare (detail and Graphical)	✓	✓
Default Demo designs	✓	✓
Extended Preferences	✓	✓
Import/Export & Search		
Intelligent interactive PDF creation for design review & comment (no editing)	✓	✓
Export ISCF (Intel Schematic Connectivity Format)	✓	✓
Export / Import XML	✓	✓
Altium Importer Schematic (PCB also available)	✓	✓
Eagle Importer Schematic (PCB also available)	✓	✓
Component Information System	CIS option	CIS option
Windows ODBC compatible format	CIS option	CIS option
Interface to relational database and management systems	CIS option	CIS option
Database query for part selection and parametric properties	CIS option	CIS option
Schematic and BOM Variants Manager (Parts not Fitted and more)	CIS option	CIS option
In-design real-time part search (DIGIKEY, FARNELL, FUTURE, MOUSER, ARROW)	CIS & CIP options	CIS & CIP options

PCB Editor	Standard	Pofessional
Layout, Placement & Routing		
Real-Time Component Placement Vision	-	NEW in QIR 7
Real-Time Route Vision	-	NEW in QIR 7
Physical, Spacing, Same net, Netclass and Class to Class rules	✓	✓
Dynamic pad suppression / Unused Pad removal	✓	✓
Cross Section Editor	✓	✓
Padstack Editor IPC2581 Compliant	✓	✓
Application Mode (General, Etch, Placement)	✓	✓
Application Mode (shape)	✓	✓
Full Skill Support	✓	✓
Customisable Visibility Pane	✓	✓
Dynamic Shape Pin Connection By Layer (Global/Shape/Pin/Layer)	✓	✓
Dynamic Cross Hatch Shapes	✓	✓

Dynamic Shapes (dynamic copper pours) Plow and Heal	✓	✓
Move with autoroute adjust (Slide)	✓	✓
Multiple placement options, manual, quickplace, auto and room	✓	✓
Aligment x and y for components and modules	✓	✓
Dynamic rat suppression	✓	✓
Fan-out generators	✓	✓
Interactive Routing using Working Layer (layer selection popup)	✓	✓
Group route Bus Route and via patterns	✓	✓
Line Fattening	✓	✓
Differential Pair Static Phase Control rules	✓	✓
Differential Pairs Physical rules and routing	✓	✓
Blind Buried Single Click multiple via instantiation	✓	✓
Push, Shove and Hug interactive editing	✓	✓
Curve Routing	✓	✓
Snake Routing for Hex pattern ICs	✓	✓
Auto Finish (Route Completion Tool)	✓	✓
Scribble Sketch Routing	✓	✓
Route cleanup, optimization (Glossing)	✓	✓
Embedded net names	✓	✓
Split View	✓	✓
Through Board Transparency (OpenGL)	✓	✓
Flip Board	✓	✓
Excellon NC Drill File export	✓	✓
Gerber 274X, 274D artwork Output	✓	✓
IPC2581 Import / Export	✓	✓
Mentor ODB++ and universal viewer	✓	✓
Impedance Calculator	✓	✓
Interactive / Automatic Silkscreen generation	✓	✓
3D/2D Crossprobing	✓	✓
STEP 3D Clash Detect	✓	✓
STEP 3D viewer for selected item or complete PCB.	✓	✓
STEP 3D In/Out	✓	✓
Manual Design For Test (DFT) / Test Prep	✓	✓
Associative Dimensioning	✓	✓
Net Scheduling, T-Point rules (pin to T-point), T-Point definition	✓	✓
Constraint Regions, region based rules (Rigid-Flex; BGA regions)	-	✓
Propagation delay rules (Relative) for nets or groups	-	✓
Propagation delay rules (Min/Max) for nets or groups	-	✓
Total Etch Length - Max/Min Length	-	✓
Extended (X)net rules	-	✓
Layer set rules	-	✓
Pin Pair rules	-	✓
Delay Tuning	-	✓
Dynamic Heads-up Display for critical rules	-	✓
Hug Contour routing (Flex)	-	✓
Segment over void detection	-	✓
Spread lines between voids	-	✓
Shape based curve fillet support, tapered traces	-	✓
Placement replication, template based design reuse	-	✓
Via array / Shielding - Shape and Trace based	-	✓
Rigid Flexi Zone Management	-	
Dynamic Zone Placement	-	✓
Inter Layer Checks for Rigid Flex	-	✓
Rigid-Flex 3D Bending	-	✓
Backdrilling	-	NEW in QIR 7
Automatic Design For Test (DFT) / Test Prep	-	-
Max Via Count rules	-	-
Offset Routing	-	-

Design planning - Create hierarchical Bundles	-	✓
Design planning - Create, Edit Flows	-	-
Design planning - Assign Flows to Layers	-	-
Component Lead Editor	-	-
Dynamic Shape based curve fillet support, tapered traces	-	-
CAD Translators - Import Mentor Boardstation	-	-
High Speed Return Path DRC	-	-
High Speed IR Drop Analysis Workflow (load capability)	-	-
High Speed Reflection Analysis Workflow (load capability)	-	-
Automatic Delay Tune (AiDT)	-	-
Automatic Phase Tune (AiPT)	-	-
Remove Tuning	-	-
Timing Vision (Coloured tracks based on constraint adherence)	-	-
Tabbed Routing	-	-
Electrical Constraint rule set (ECSets) / Topology Apply	-	-
Electrical rules (Reflection, Timing, Crosstalk)	-	-
Advanced Constraints (formulas, relational)	-	-
Fabric Weave Effect Zig Zag Auto Interactive	-	-
High Speed Static Phase Via Transition DRC	-	-
Via Voiding Differential Pairs	-	-
Single net Return Paths Vias	-	-
High Speed Differential Pair Return Path Vias	-	-
High Speed Intra Differential Pairs Spacing Rules	-	-
High Speed Via Structures	-	-
High Speed Inductance Via Structures	-	-
Constraint Manager: HDI rule set	-	-
Micro-via and associated spacing, stacking and via-in-pad rules	-	-
Constraint driven HDI design flow	-	-
HDI micro-via stack editing	-	-
Manufacturing rule support for embedding components	-	-
Embed components on inner layers	-	-
Support for Cavities on inner layers	-	-
Support for Vertically placed components on inner layers	-	-
Soldermask for embedded components	-	-
Support for copy and swap embedded components	-	-
Dual Side Contact Embedded Components	-	-
Design Planning - Plan Spatial Feasibility analysis & feedback	-	-
Design Planning - Generate Topological Plan	-	-
Design Planning - Convert Topological plan to traces (CLINES)	-	-
Auto Interactive Break-out (AiBT)	-	-
Auto Connect (Breakout, Connect, Compress, Spread, Nudge, Push)	-	-
Symphony Team Design New Option	-	-
Concurrent Team Design - Layer by Layer	-	-
Concurrent Team Design - Functional block partitioning	-	-
Concurrent Team Design - Team design dashboard	-	-
Concurrent Team Design - Soft boundaries	-	-
Concurrent Team Design - Constraint Editing and Netclasses per Partition	-	-
Swap pins on a FPGA (based on FPGA rules) in PCB Editor	-	-
Reoptimize pins on a FPGA (using FPGA rules)	-	-
Parameterized RF etch elements	-	-
Asymmetrical Clearances	-	-
RF Etch elements editing	-	-
Bi-Directional interface with Agilent ADS	-	-
ADS schematics Import Agilent into DE-HDL	-	-
Layout-driven RF design creation	-	-
Flexible Shape Editor	-	-
PCB Signal Integrity (Coupling, Impedance, Timing) Analysis		

Real-Time High Speed Analysis Impedance Workflow	-	NEW in QIR 7
Real-Time High Speed Analysis Coupling Workflow	-	NEW in QIR 7
Real-Time Differential Pair Dynamic Phase Control rules	-	NEW in QIR 7
Real-Time Package Pin Delay (for die-2-die delay) rules	-	NEW in QIR 7
Real-Time Z-Axis delay feedback	-	NEW in QIR 7
Pre- & Post-route signal integrity analysis	Pre Route	✓
Graphical topology definition and exploration	Pre Route	✓
Interactive waveform viewer	Pre Route	✓
Macro modelling support (DML)	Pre Route	✓
IBIS 5.0 support	Pre Route	✓
IBIS ICM model support	Pre Route	✓
Spectre-to-DML	Pre Route	✓
HSPICE-to-IBIS	Pre Route	✓
Lossy transmission lines	Pre Route	✓
Coupled (3 net) simulation Pre-Route	Pre Route	✓
Differential pair exploration and simulation	Pre Route	✓
PCB Auto-Router		
6 Signal Layers at a time (no board layer limit or pin limit)	-	✓
Shape-based or Gridded routing	-	✓
SMD Fanout	-	✓
Physical Trace Width by Net and Net Classes	-	✓
45-degree / Memory Pattern Routing	-	✓
Interactive Routing with Shoving and Plowing	-	✓
Interactive Floorplanning	-	✓
Online Design Rule Checking	-	✓
Flip, Rotate, Align, Push, and Move Components	-	✓
Placement Density Analysis	-	✓
Min/Max, matched length rules based autorouting	-	-
Pin-pair rules, Area rules based autorouting	-	-
Crosstalk controls, parallelism rules based autorouting	-	-
Differential Pair Autorouting, Automatic net shielding	-	-
High-speed rules-based autorouting	-	-
256 signal layer limit	-	OrCAD AI Option
DFM rules-based autorouting automatic trace spreading, via reduction and mitering	-	-
Spacing Net Class - Class Rules	-	-
Via Rules by Net and Net Class	-	-
Mircovia features including Plural and Stacked microvias	-	-
Auto Test Point Generation and Clearance Rules	-	-
Layer-specific rules-based autorouting	-	-
Design For Manufacturability Checks (DFM & DRC)		
DesignTrue DFM Wizard	NEW in QIR 7	NEW in QIR 7
Design for Test Checks	NEW in QIR 7	NEW in QIR 7
Design For Assembly Checks	NEW in QIR 7	NEW in QIR 7
Design For Fabrication Checks	NEW in QIR 7	NEW in QIR 7
Manufacturing DFX Rules	✓	✓
Component Height DRC	✓	✓
DFM Checks including soldermask, solderpaste and more	✓	✓
DFM Pad Entry / Exit Rules	✓	✓
Import/Export Formats Supported		
Import File Manager	✓	✓
Import Altium PCB (schematic also available)	✓	✓
Import EAGLE PCB (schematic also available)	✓	✓
Import PADS & PCAD	✓	✓
Import IFF RF Shapes	✓	✓
Import Export DXF	✓	✓
Import Export IDF	✓	✓
MCAD/ECAD Incremental design data exchange (IDX)	✓	✓
Export PDF	✓	✓